IN THE CLAIMS

What is claimed is:

1. A data processing apparatus that arbitrates sharing of a single semiconductor memory circuit among multiple data processing circuits, comprising:

a semiconductor memory circuit that executes operations corresponding to a command signal, address signal and clock signal received external to the semiconductor memory circuit; and

a data processing circuit that supplies the semiconductor memory circuit with a clock enable signal for enabling an input of the clock signal when active and a disabling the input of the clock signal when inactive, and a chip select signal for enabling input of command signals when the chip select signal is active and disabling input of command signals when the chip select signal is inactive; wherein

before the data processing circuit ends control of the semiconductor memory circuit and stops supplying the clock enable signal and chip select signal, a different data processing circuit starting control of the semiconductor memory circuit supplies a clock enable signal and chip select signal values at the same state as those provided by the data processing circuit ending control of the semiconductor memory circuit.

2. The data processing apparatus of claim 1, wherein:

the data processing circuit supplies a sharing arbitration circuit with a

request when requesting control of the semiconductor memory circuit, controls the semiconductor memory circuit in response to a grant signal, and supplies the arbitration circuit with a busy signal while controlling the semiconductor memory circuit;

when ending control of the semiconductor memory circuit, the data processing circuit stops supplying the clock enable signal and chip select signal a predetermined time after stopping the supply of the busy signal; and

the sharing arbitration circuit generates the grant signal in response the request signal before the predetermined time has elapsed.

3. The data processing apparatus of claim 1, wherein:

the semiconductor memory circuit enters a lower power state when the clock enable signal is inactive, as compared to when the clock enable signal is active.

4. The data processing apparatus of claim 1, wherein:

one of the multiple data processing circuits is a master device while any others are slave devices; and

the master device supplies the clock enable signal and chip select signal to the semiconductor memory circuit when none of the slave devices provides the clock enable signal and chip select signal to the semiconductor memory circuit.

5. The data processing apparatus of claim 1, wherein:

the multiple data processing circuits are connected to one another but formed independently of one another.

6. The data processing apparatus of claim 2, wherein:

one of the multiple data processing circuits is a master device while any others are slave devices; and

the sharing arbitration circuit is built into the master device.

7. The data processing apparatus of claim 1, wherein:

each of the data processing circuits of the multiple data processing circuits includes a built in sharing arbitration circuit;

the multiple data processing circuits are initialized to establish one data processing circuit as a master device and all others as slave devices; and

the arbitration circuit of the master device is enabled and the arbitration circuits of the slave devices are disabled.

8. The data processing apparatus of claim 7, wherein:

in an initialization operation, the sharing arbitration circuit built into the master device supplies at least one slave device with a grant signal; and

the at least one slave device supplies a request signal of a predetermined time period if the grant signal is received while the slave device is not supplying its own request signal; wherein

the sharing arbitration circuit built into the master device stops supplying the grant signal once the startup of the at least one slave device is confirmed by input of the request signal from the at least one slave device.

9. A data processing apparatus, comprising:

a semiconductor memory circuit that is controlled by inputs to at least one control input;

at least one control line coupled to the control input of the semiconductor memory circuit; and

a plurality of data processing circuits that share access to the semiconductor memory circuit, each having a control output coupled to the control line; wherein

when one data processing circuit ends control of the semiconductor memory circuit, the data processing circuit provides a control signal at the control output at a predetermined potential for a first time period before ending the control signal; and

when one data processing circuit starts control of the semiconductor memory circuit, the data processing circuit provides a control signal at its control output at the predetermined potential within the first time period.

10. The data processing apparatus of claim 9, wherein:

the semiconductor memory circuit operates in synchronism with a clock signal, and the at least one control input includes

a chip select input that enables the processing of commands by the semiconductor memory circuit, and

a clock enable signal that enables generation of timing signals within the semiconductor memory circuit.

11. The data processing apparatus of claim 9, wherein:

each of the plurality of data processing circuits includes

a request input/output (I/O) for indicating when the data processing circuit seeks control of the semiconductor memory circuit,

a grant I/O for indicating when the data processing circuit is granted control of the semiconductor memory circuit, and

a busy I/O for indicating when the data processing circuit is controlling the semiconductor memory circuit.

12. The data processing apparatus of claim 11, wherein:

each of the plurality of data processing circuits includes

a first switch for selectively connecting the request I/O, grant I/O, and busy I/O to a requesting circuit that generates a request indication and busy indication for the data processing circuit, and

a second switch for selectively connecting the request I/O, grant I/O, and busy I/O to an arbitration circuit that generates a grant indication; wherein

the first switch is disabled and the second switch is enabled

when the data processing circuit is initialized as a master device, and the first switch is enabled and the second switch is disabled when the data processing circuit is initialized as a slave device.

13. The data processing apparatus of claim 12, wherein:

each data processing circuit includes

a controller that generates at least one controller signal for enabling or disabling the first switch and second switch according to initialization data.

14. The data processing apparatus of claim 9, wherein:

the at least one control line is directly connected to the control input of the semiconductor memory circuit and the control output of each of the plurality of data processing circuits.

15. A method of sharing a semiconductor memory circuit with a plurality of data processing circuits, comprising the steps of:

when a data processing circuit ends control of the semiconductor memory circuit, driving control outputs coupled to control lines for the semiconductor memory circuit to predetermined logic values, and subsequently placing the control outputs in a high impedance state; and

when a data processing circuit starts control of the semiconductor memory circuit, driving control outputs coupled to control lines to the

predetermined logic values prior to the control outputs of the semiconductor device that is ending control of the semiconductor memory circuit being placed in the high impedance state.

16. The method of claim 15, wherein:

the semiconductor memory circuit and data processing circuit operate in synchronism with a clock signal;

when the data processing circuit ends control of the semiconductor memory circuit, the data processing circuit places the control outputs in the high impedance state a first number of clock cycles after ceasing operating with the semiconductor memory circuit; and

when the data processing circuit starts control of the semiconductor memory circuit, the data processing circuit drives control outputs to the predetermined logic values a second number of clock cycles after the data processing circuit that is ending control ceases operating with the semiconductor memory circuit; wherein

the second number of clock cycles is less than the first number of clock cycles.

17. The method of claim 16, wherein:

the second number of clock cycles is one and the first number of clock cycles is two.

18. The method of claim 15, further including:

when a data processing circuit initializes as a master device, the data processing circuit outputs a grant control signal; and

when a data processing circuit initializes as a slave device, the data processing circuit outputs a request signal, having a predetermined duration, after receiving a grant signal from the master device, and places control outputs in the high impedance state.

19. The method of claim 15, wherein:

when the data processing circuit ends control of the semiconductor memory circuit, the data processing circuit sets a busy signal to an inactive state, and subsequently places the control outputs in the high impedance state.

20. The method of claim 15, wherein:

when the data processing circuit seeks control of the semiconductor memory circuit, the data processing circuit activates a request signal, and if a corresponding grant signal is activated, the data processing circuit subsequently drives control outputs to the predetermined logic values.